

**REMARKS**

Claims 1-5 and 7-9 are pending in the application.

Claims 3 and 4 have been amended solely to correct informalities.

Claim 8 has been canceled.

Claims 1-5, 7 and 9 have been allowed.

Reconsideration of the claims is respectfully requested.

**I. CLAIM REJECTIONS -- 35 U.S.C. § 102**

Claim 8 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,522,192 to *Sander* (hereinafter “*Sander*”). This rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Independent Claim 8 recites “a boost converter having voltage selectable modes, the boost converter comprising a first selection terminal and a second selection terminal.” The claim also recites “a capacitive boost circuit, wherein the capacitive boost circuit is utilized in a capacitive mode.” The claim further recites “an inductive boost circuit, wherein the inductive boost circuit is

utilized in an inductive mode; and a mode selection circuit, wherein the mode selection circuit selects the capacitive mode if a voltage source is connected to the first selection terminal and selects the inductive mode if the voltage source is connected to the second selection terminal.”

The Applicant respectfully maintains the arguments presented in the last response. The Applicant submits that *Sander* does not disclose a mode selection circuit, wherein the mode selection circuit selects the capacitive mode if a voltage source is connected to the first selection terminal and selects the inductive mode if the voltage source is connected to the second terminal as recited by Claim 1.

*Sander* teaches a boost doubler circuit wherein switches (SW3 and SW2) are turned on to introduce a deliberate overlap of the clock such that both the inductive component and capacitive component operate at the same time. (*Sander*, col. 2, lines 40-64). *Sander* contains no disclosure for selecting of modes. *Sander* (T1) describes a first clock and (T2) describes a second clock. However, *Sander* (Figure 5) illustrates a deliberate overlapping of the clock signals.

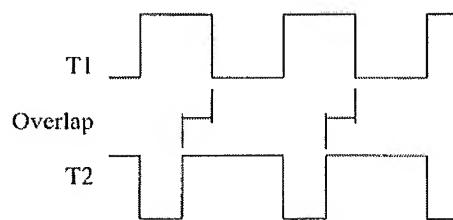


Fig. 5

*Sander* teaches, and is limited to teaching, a boost circuit configured to have both the inductive component and capacitive component operate at the same time. *Sander* does not teach a mode selection. Therefore, *Sander* does not contemplate “a mode selection circuit, wherein the mode selection circuit selects the capacitive mode if a voltage source is connected to the first selection terminal and selects the inductive mode if the voltage source is connected to the second terminal” as arranged and recited by Claim 1

However, in order to further prosecution, the Applicant has canceled Claim 8, without prejudice.

## II. ALLOWABLE SUBJECT MATTER

The Applicant thanks the Examiner for allowing Claims 1-5, 7 and 9.

**CONCLUSION**

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

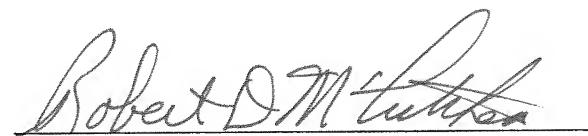
If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at [rmccutcheon@munckcarter.com](mailto:rmccutcheon@munckcarter.com).

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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